Implementation of a Carry Look-Ahead Adder circuit using Reversible Logic

Naman Sharma
Bharati Vidyapeeth's College of Engineering, New Delhi-110063

Namansharma14692@gmail.com

Upanshu Saraswat
Bharati Vidyapeeth's College of Engineering, New Delhi-110063

upanshusaraswat@gmail.com

Rajat Sachdeva
Bharati Vidyapeeth's College of Engineering, New Delhi-110063

rajat.sachdeva621@gmail.com

Abstract— Conventional irreversible gates have been firmly established to have a loss of energy equal to kT ln(2) joule per lost bit. This is due to the loss of information at every gate that has unequal number of inputs and outputs. Reversible logic based technologies provide a way around these losses. Reversible logic is highly useful in nanotechnology, low power design and quantum computing. This paper proposes a design for a faster adder using reversible gates.

Keywords: Reversible logic, Adders, Carry look-ahead Adder, Quantum computing.

— — — — — — — — — ◆ — — — — — — — — —

1. INTRODUCTION

With the advent of new technology, better fabrication techniques and better floor plan designs, devices have become increasingly smaller. The recent advancements in the field of Large Scale Integration, especially over the last ten years have enabled us to create new, more powerful devices than ever before. Our technology has become ever more portable, personalized and have tremendous built-in functionality. With the size of the chip being reduced, power consumption has become the paramount concern during design considerations. There is constant research in the field of low power electronics where there is an attempt to find ways to minimize power consumption as much as possible [11].

It is predicted that the Moore's law is at an end due to the inability of the designers to keep up with the power requirements of the future chips [1]. One of the solutions to meet the low-power requirement of the future devices is by adopting an entirely new model known as Reversible Logic. Reversible logic finds its origins in the concepts of Quantum Computing [12]. Researchers like Bennett showed that the devices based on reversible computing consume much less power than the traditional irreversible devices [3] [4]. Reversible logic gates use one-to-one mapping between input and output vectors, thereby preventing loss of information, which in turn results prevents dissipation of energy, as shown by Landauer [5] [6]. A large number of circuits (both combinational and sequential) using reversible logic, have been proposed in literature. This paper seeks to implement a faster adder circuits using reversible logic gates.

Toffoli demonstrated in [13] that reversible logic structures are satisfactory for design and implementation in computing structures and organization when those design rules ensure the logic structure is invertible. Deustch later stated that reversible gates connected to each other by means of unit wires can be sufficiently used for the generation of a quantum computational network [15] [14]. Quantum (reversible) gates are the generalization of classical logic gates. Deustch defined a source bit of '0' or '1' as a gate which, once every computational step, produces a value of '0' or '1' on its output [15]. He argued that the source bits are reversible gates, since there was a bi-jective relationship observed between the value produced at the gate input, and the produced output. Since fast computational speed and power efficiency are among the foremost considerations during design considerations, therefore it was the aim of the authors to implement a faster adder (using the look-ahead carry scheme).

The paper begins by briefly describing the concept and applications of the reversible logic in section 2. In section 3, the authors have described the concept of reversible logic gates, and have summarized some of the most popular reversible gates. Section 4 of the paper talks about the look ahead carry adder, and its requirement in modern circuits. Further, this section also describes the architecture of the design for a full adder as proposed by the authors. The simulation for the functional correctness of the given circuit is performed in ModelSim and the hardware is described using a Verilog code. Section 5 gives the waveforms generated by the circuit in order to check whether it has been implemented correctly and Section 6 concludes the paper.

2. REVERSIBLE LOGIC

A circuit/gate is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments [24]. The most prominent application of reversible logic is found in the generation of quantum computers [22]. Any quantum computer can be considered as a network (or a family of networks) composed of quantum logic gates; therefore each reversible gate is the basic building block for the said network. It has applications in various research areas such as Low Power device design and quantum computing.

Quantum networks have been established to be composed of quantum logic gates; each gate performing a basic elementary unitary operation on one, two or more than two–state quantum systems called qubits. Each qubit represents an elementary unit of information; corresponding to the classical bit values 0 and 1

[23]. Any unitary operation is reversible and hence quantum networks effecting elementary arithmetic operations such as addition, multiplication and exponentiation cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible).Thus, quantum arithmetic must be built from reversible logical components [22]. Reversible computation in a system can be performed only when the system comprises of reversible gates.

3. BASIC REVERSIBLE GATES

In 1960, researcher R. Landauer demonstrated that circuits using irreversible hardware results in energy dissipation of kTln2 Joules due to one bit loss of information where k is Boltzmann's constant and T the absolute temperature [5][6]. Bennett showed that this energy loss can be avoided by constructing circuits using reversible logic gates [3][4] . A reversible logic gate is an n-input, n-output logic function that maintains a one-to-one mapping between the two. Based on this principle, different basic reversible gates such as Feynman [7], Toffoli [8] and Peres [10] have been proposed. A 2*2 Feynman gate with inputs (A,B) produces the output P equal to input A while output Q as the XOR of the inputs [18]. A 3*3 Toffoli gate with inputs (A, B, C) and outputs (P, Q, R). It has outputs P and Q equal to A and B respectively while the output R is complement of the input C if both A and B are at logic 1, otherwise it is input C [21] [19] . A Fredkin gate is a 3*3 gate with inputs A, B and C giving outputs P, Q and R. The outputs are defined as P = A; Q= A'B + AC; and R= AB + A'C [20]. A Peres gate is a 3*3 reversible gate with inputs (A, B, C) and outputs (P, Q, R). The output P is equal to A; output Q is the XOR of A and B while R is complement of the input C if both A and B are equal to 1, otherwise it is equal to input C [21]. A URG gate is a 3*3 gate with inputs (A, B, C) and outputs P= (A+B) xor C, Q= B, R = AB xor C [18].

4. CARRY LOOK-AHEAD ADDER

Delays in a circuit may be caused due to a variety of reasons. The primary shortcoming of a ripple carry adder is the fact that at every bit must wait for the result of the previous carry. This is a significant impediment for circuit speed. Each bit waits for the carry generated at the previous bit, in order to calculate the next sum. This causes delays in the circuit. In contrast, the carry look-ahead adder block, calculates the next carry bit with the sum. Due to this, the current bit already has the value of the carry, required to calculate the sum. This significantly improves speed, and reduces delays in the circuit. The block diagram implementation of a carry look ahead block is as given below.
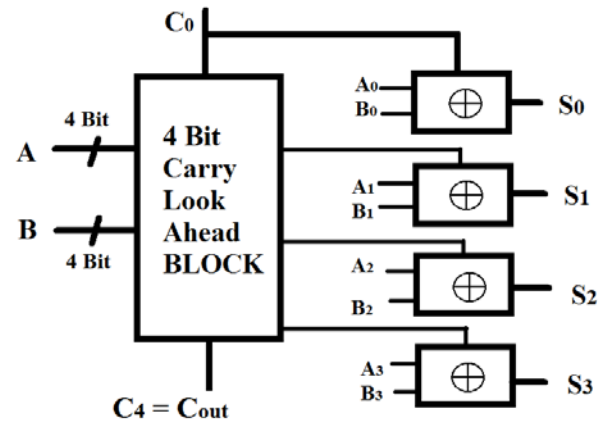

Fig 1: Block diagram representing a carry look ahead adder circuit

The most critical component of this adder is the carry look ahead block. It performs the task of simultaneously calculating the carry, so that there need not be any delay in receiving carry from the previous bit. This enables faster computation and the inherent quality of reversible logic based circuits make it a lucrative option for circuit designers.

The carry look ahead block handles the carry in two different ways namely, carry generated (G) and carry propagated (P). For the ith bith is given denoted as C_i. From Boolean algebra it can be easily calculated that C_i is given by:

$$C_{i+1} = G_i + P_i \qquad \ldots (1)$$

where,

$$G_i = A_i \cdot B_i \qquad \ldots (2)$$

$$P_i = A_i \oplus B_i \qquad \ldots (3)$$

Hence for a 4-Bit implementation,

$$C_1 = G_0 + P_0.C_0 \qquad \ldots (4)$$

$$C_2 = G_1 + P_1.C_1 \qquad \ldots (5)$$

$$C_3 = G_2 + P_2.C_2 \qquad \ldots (6)$$

$$C_4 = G_3 + P_3.C_3 \qquad \ldots (7)$$

With this information, we can implement the carry look ahead block using reversible gates as follows.

As it can be seen from the diagram below, a look ahead carry unit can be used to generate the carry from previous bits simultaneously. Hence it substantially reduces circuit delays. These carries that have been generated (namely C_1, C_2, C_3, C_4) need to be further combined with the inputted bits A and B to give the sum of these two numbers. This is given by,

$$S_i = A_i \oplus B_i \oplus C_i \qquad \ldots (8)$$

And hence,

$$S_0 = A_0 \oplus B_0 \oplus C_0 \qquad \ldots (9)$$

$$S_1 = A_1 \oplus B_1 \oplus C_1 \qquad \ldots (10)$$

$$S_2 = A_2 \oplus B_2 \oplus C_2 \qquad \ldots (11)$$

$$S_3 = A_3 \oplus B_3 \oplus C_3 \qquad \dots (12)$$
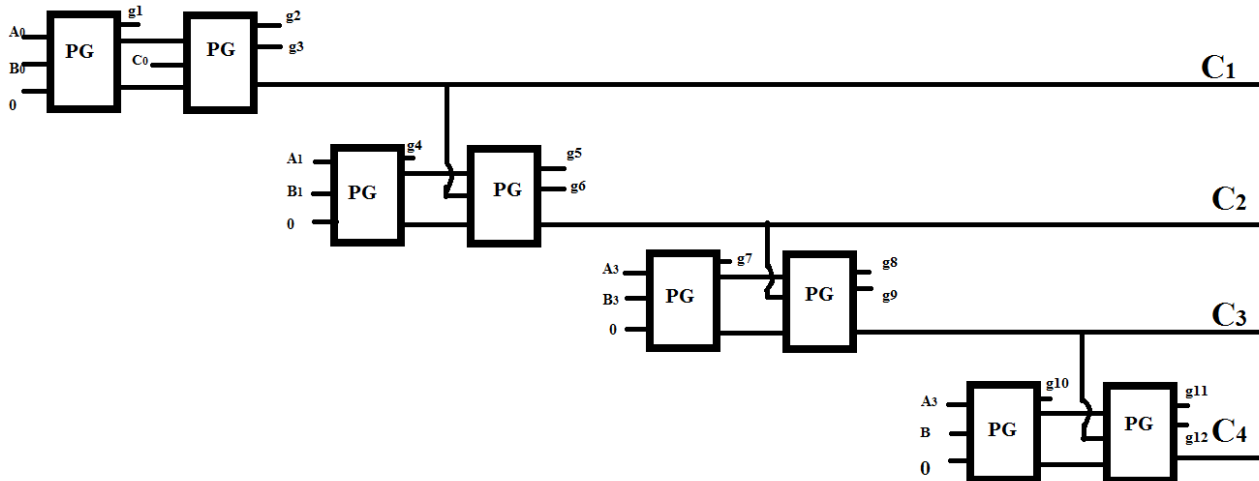

Fig 2: Implementation of a look-ahead carry unit using Reversible Logic Gates (Peres Gates)

Hence the adder can be implemented using the above equations by giving the outputs of the look ahead carry unit as inputs to the TKS gate, combined along with external inputs A and B. This is achieved by the following architecture.
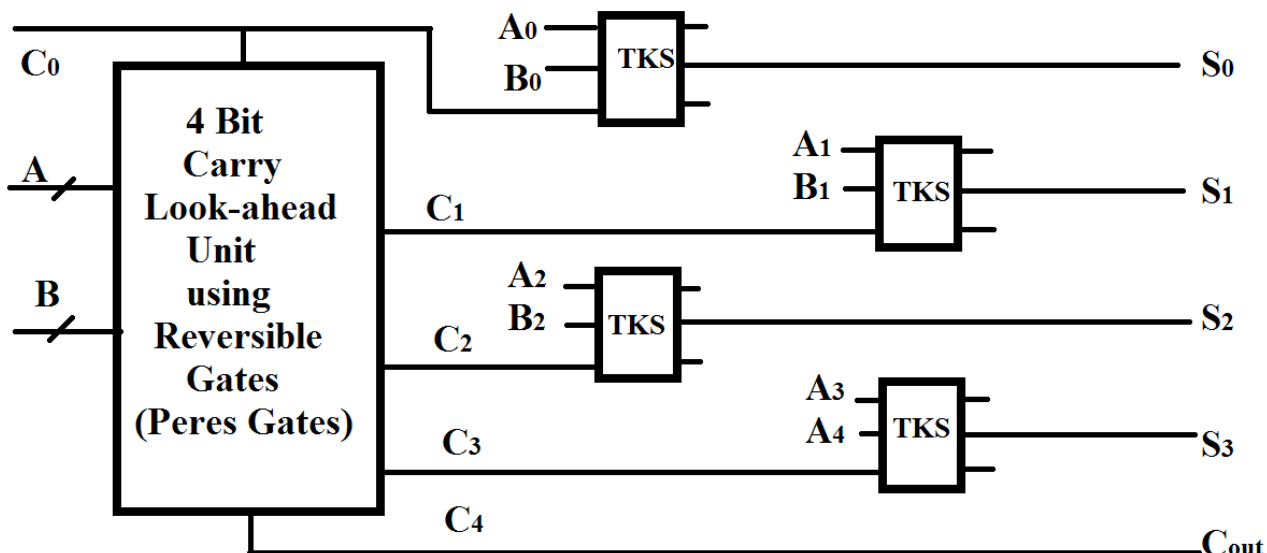

Fig. 3: Implementation of a 4-Bit Look-ahead carry adder using reversible logic gates (Peres and TKS)

The functional verification for the given circuit was performed using ModelSim too. Verilog code was written for the proposed architecture and the waveforms generated for the same, in order to check functional correctness. It was found that the adder worked perfectly for the given test cases.
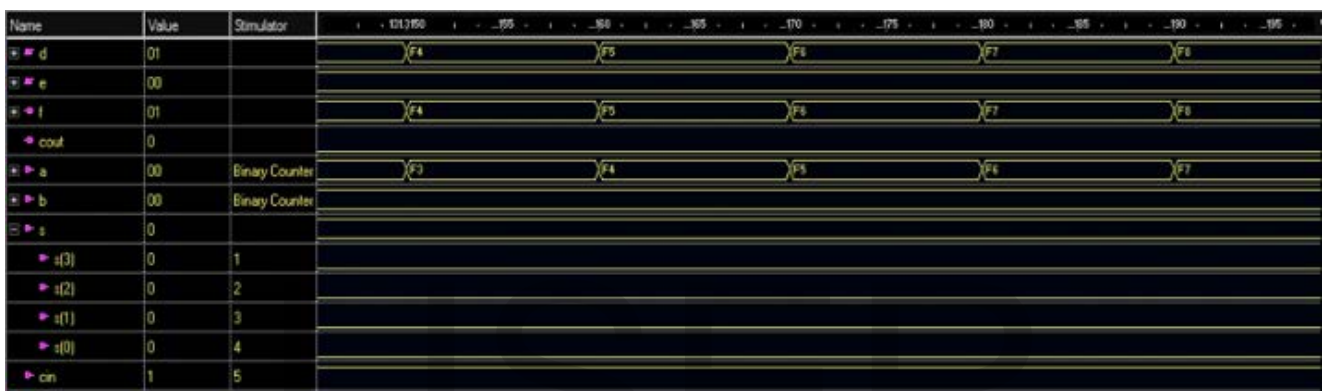
5. SIMULATION SECTION

Fig 4. Waveform analysis of the carry look-ahead adder circuit

6. CONCLUSION

The use of reversible logic based technologies is a promising choice for creating computational devices in the future. With quantum computing using Reversible Logic as the building blocks for the future computers, one can safely assume that such technologies will be critical in the near future. These circuits provide effective, power efficient alternatives to the modern day digital computers. They also provide significantly less number of garbage outputs as compared to other digital circuits.

In addition circuits that can provide solutions to delay problems in the hardware design of the circuit, like the one we proposed above can help us design faster and more power efficient devices. These are the two most important considerations for all design engineers, and the authors believe that the use of reversible gates will be critically important in future technologies.

7. REFERENCES

[1] Laszlo B. Kish, Texas A&M University, Department of Electrical Engineering, College Station, TX 77843-3128, USA Received 16 July 2002; received in revised form 19 September 2002; accepted 19 September 2002, Communicated by C.R. Doering, "End of Moore's law: thermal (noise) death of integration in micro and nano electronics."

[2] Trevor Pering, Tom Burd, and Robert Brodersen University of California Berkeley, Electronics Research Laboratory, "Dynamic Voltage Scaling and the: Design of a Low-Power Microprocessor System"

[3] C. H. Bennett, "Notes on the history of reversible computation," IBM J. Research and Development, vol. 32, pp. 16-23, January 1988.

[4] C. H. Bennett, "Logical reversibility of computation," IBM J. Research and Development, pp. 525-532, November 1973.

[5] R. W. Keyes and R. Landauer, "Minimal energy dissipation in logic," IBM J. Research and Development, pp. 152-157, March 1970.

[6] R. Landauer, "Irreversibility and heat generation in the computing process," IBM J. Research and Development, vol. 3, pp. 183-191, July 1961.'
.

[7] R. Feynman," Quantum Mechanical Computers", Optic News, Vol 11, pp 11-20 1985.

[8] T.Toffoli, "Reversible Computing", Tech memoMIT/LCS/TM-151, MIT Lab for Computer Science 1980.

[9] Fredkin E. Fredkin and T. Toffoli,, "Conservative Logic", Int'l J. Theoretical Physics Vol 21, pp.219-253, 1982

[10] Peres, "Reversible Logic and Quantum Computers", Physical review A, 32:3266- 3276, 1985.

[11] Padmanabhan Pillai and Kang G. Shin, "Real-Time Dynamic Voltage Scaling for Low-Power Embedded Operating Systems", Real-Time Computing Laboratory Department of Electrical Engineering and Computer Science The University of Michigan Ann Arbor, MI 48109-2122, U.S.A.

[12] Asher Pers, "Reversible logic and quantum computers", The American Physical Society

[13] T. Toffoli, "Reversible Computing," Technical Report MIT/LCS/TM-151, 1980.

[14] D. Deutsch, "Quantum Theory, the Church-Turing Principle and the Universal Quantum Computer," Proceedings of the Royal Society of London, vol. 400, 1982.

[15] D. Deustch, "Quantum Computational Networks," Proceedings of the Royal Society of London. Series A, Mathematical and Physical Sciences , vol. 425, iss. 1868, 1989, pp. 73-90

[16] A Novel Quantum Cost Efficient Reversible Full Adder Gate in Nanotechnology Md. Saiful Islam Institute of Information Technology, University of Dhaka, Dhaka-1000, Bangladesh

[17] V. Rajmohan, Member IACSIT, V. Renganathan, and M. Rajmohan ―A Novel Reversible Design of Unified Single Digit BCD Adder-Subtractor‖, International Journal of Computer Theory and Engineering, Vol. 3, No. 5, October 2011

[18] Md. Belayet Ali , Md. Mosharof Hossin and Md. Eneyat Ullah, ―Design of Reversible Sequential Circuit UsingReversible Logic Synthesis‖ International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.4, December 2011

[19] Fredkin E. Fredkin and T. Toffoli,‖Conservative Logic‖, Int'l J. Theoretical Physics Vol 21, pp.219-253, 1982

[20] Peres, ―Reversible Logic and Quantum Computers‖, Physical review A, 32:3266- 3276, 1985.

[21] Vlatko Vedral, Adriano Bareno and Artur Ekert, ―QUANTUM Networks for Elementary Arithmetic Operations‖, arXiv:quantph/ 9511018 v1, nov 1995

[22] M. Mohammadi and M. Eshghi. On figures of merit in reversible and quantum logic designs. Quantum Information Processing, 8(4):297–318, Aug. 2009.

[23]Perkowski, M., A. Al-Rabadi, P. Kerntopf, A. Buller, M. Chrzanowska-Jeske, A. Mishchenko, M. Azad Khan, A. Coppola, S.Yanushkevich, V. Shmerko and L. Jozwiak, ―A general decomposition for reversible logic‖, Proc. RM'2001, Starkville, pp: 119-138, 2001..

IJSER